# RF POWER DETECTOR USING A SILICON MOSFET

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**Abstract**
This paper presents a novel approach for RF power measurements using a *silicon MOSFET* . It describes linear and nonlinear models of the RF MOSFET for results prediction. It shows a thorough comparison between predicted and measured results. The detector demonstrates a better sensitivity than biased Schottky diode detectors that we have measured.

**Introduction**
The needs for robust and low cost technologies for RF applications have increased the activity in silicon MOS transistor research, while most of this activity has been in the power amplification areas, this paper will demonstrate the RF capabilities of s*ilicon MOSFETs* beyond power amplifiers and will discuss how MOS transistor can be used in RF power detection.
To our knowledge there are no previously published results concerning RF power measurements using silicon MOSFETs. However, Krekels et al [1] have presented a GaAs MESFET power detector using a physical model transistor (Shockley's theory), but no predicted results have been presented. Boulouard [2] has used a cold GaAs MESFET model from the Philips foundry and has compared only the measures and simulated values of the detectors' Sij parameters.
This paper presents a silicon MOSFET and its linear and non linear models for RF power measurements purpose. After that, the measured and predicted results are compared. In RF technologies it is common to use a biased Schottky diode for power measurements [3-4]. The diode causes a deformation of the RF signal due to its nonlinear current voltage characteristic. Thermistors are also used in RF power measurements, their major drawback is that they require high RF power signals due to their low sensitivity.
Field effect transistors provide also a nonlinear current voltage I-V characteristic. Thus, they can be used as RF power detector [1-2-5]. Compared to the biased Schottky diode the FET has presented a better sensitivity and the output voltage is directly available without substracting the bias voltage. FET detector is less sensitive to temperature variations than a Schottky diode detector and the effective noise voltage of the diode detector, 600 nV, is four times as high as the FET noise level [1]. All these characteristics make the FET detector a major player in the RF power measurements.

**RF power detector principles**.
The basic detector concept relies on a deformation of the RF signal with a nonlinear element. In consequence the RF signal will be decomposed in a DC signal component and a number of harmonics.

$$I = I_{dc} + Fundamental + Harmonics$$

The DC current is then a function of the RF signal amplitude. Thanks to the I-V characteristic of the nonlinear element the output voltage $V_{out}$ is proportional to the RF power signal $P_{rf}$ at low power levels: $V_{out} \propto P_{rf}$.

**MOSFET detector.**
Figure 1a-b show a design of two RF power detector structures. The nonlinear elements used are *Silicon MOS transistors* $T_1$ and $T_2$, with a gate area of 0.5*135 $\mu m^2$ biased through an RC cell at Vgs = 0.6 V.
In the first structure figure 1a. $T_1$ is a common-gate transistor, resistor $R_1$ (1 k$\Omega$) ensure that the RF isolation between DC generator and drains MOSFET is sufficient. The RF signal will be deformed through the drain-source resistance $R_{ds1}$, therefore the signal at source path is composed of a DC current and number of harmonics. The DC voltage is then available thanks to capacitor $C_1$ (10 pF) and load resistor $R_{L1}$ (10 k$\Omega$).
Transistor $T_2$ is parallel to the RF power line feed (figure 1b). It is isolated from the generator by a high pass filter constitued with a high capacitor $C_2$ (60 pF). Theoretically a low pass filter should be placed between the transistor $T_2$ and the output

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circuit RC. Due to MMICs' technology constraints this filter has been replaced by a resistance whose value (1 kΩ) is greater than the drain-source resistance $R_{ds2}$. The RF signal will then flow through the transistor. Its DC current is collected at the load resistance $R_{L2}$ (10 kΩ), the 10 pF capacitor is used as a shunt element for the remaining harmonics of the RF signal.

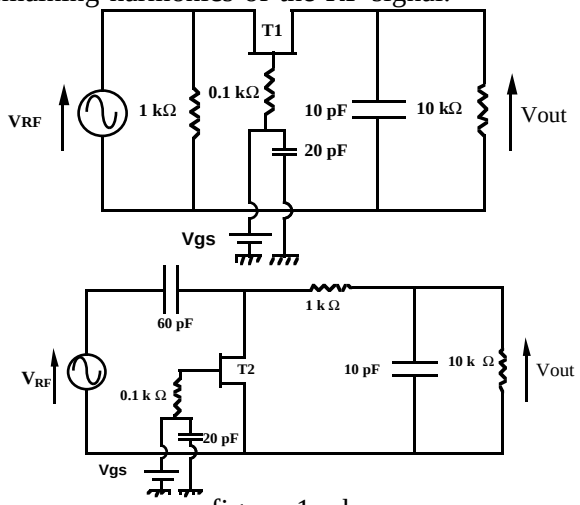



figure 1.a-b.

**RF MOSFET modelisation.**

Non linear modelisation generally starts with a linear modelisation. As the foundry doesn't provide a RF small signal equivalent circuit, we had to model the MOS transistor at low gate voltage biasing.

Figure 2 shows the schematic of the equivalent model used to characterize the small signal behavior of the silicon MOSFET. Basically this equivalent circuit can be divided into two parts:

- Extrinsic elements $R_g$, $R_s$, $R_d$, $C_{pg}$ and $C_{pd}$, which are independant of the biasing conditions.
- Intrinsic elements $G_m$, $\tau$, $R_{ds}$, $C_{gs}$, $C_{gd}$, and $C_{ds}$, which are function of the biasing conditions.

The traditional GaAs FET parameters extraction method uses either DC and cold FET AC measurements to establish the extrinsic resistances values [6]. This technique has been modified [10] because the gate of a silicon MOSFET is DC isolated from the remainder of the device.

First, the device was biased at Vgs =Vds = 0. In this way, the Z-parameters of the device are given by equations (1-3). On Wafer S-parameters measurements are down using a vectorial network analyzer. The parasitic resistances were obtained after matrix S-Z conversion.

$$Re(Z11) = Rg + Rs \quad (1) \qquad Re(Z12) = Re(Z21) = Rs \quad (2)$$

$$Re(Z22) = Rd + Rs \quad (3)$$

$$Im(Y11) = j\omega(Cpd + 2*Cb) \quad (4)$$

$$Im(Y12) = Im(Y21) = -j\omega(Cb) \quad (5)$$

$$Im(Y22) = j\omega(Cpd + Cb) \quad (6)$$

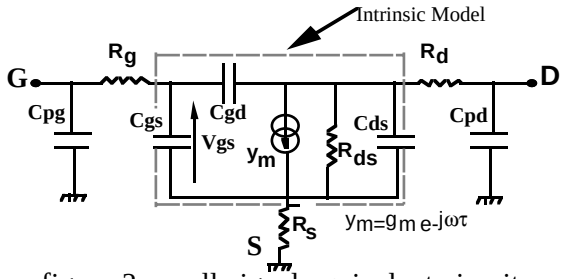



figure 2. small signal equivalent circuit.

Rg = 5.5Ω, Rs = 10Ω, Rd = 5Ω, Cgs = 0.18pF, Cgd = 0.10pF, Cds = 0.17 pF, Cpg = 0.23pF, Rds = 0.9kΩ, Cpd = 0.20pF, Gm = 9.74e-$^4$S, t = 5 e-$^{12}$ps

The input and output capacitance Cpg, Cpd are obtained by suppresing the channel conduction Vds = 0 and Vgs < Vp (pinch off voltage), In this way, the Y-parameters of the device are given by equations (4) to (6), capacitor Cb represents the fringing capacitance due to the depleted layer extension at each side of the gate.

Comparing to [10], this new method for determining the parasitic capacitance for a MOSFET take into account the gate and drain pad capacitance, it is very useful, the MOSFET model can then be characterized by means of parasitics capacitances, furthermore the intrinsic gate to source capacitance $C_{gs}$ is accurately defined. Now that the extrinsic elements have been defined, it is possible to determine the intrinsic model parameters, thus the equivalent circuit component for any gate and drain bias voltage.

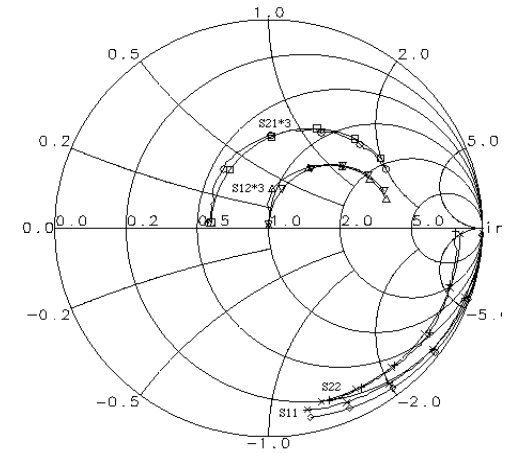
The intrinsic small signal elements can be deduced from the Y-parameters network, using a de-embeeding of the extrinsic parameters values, equation (7)-(10) give the expressions of the Y-parameters in function of the capacitances $C_{gs}$, $C_{gd}$, $C_{ds}$, $G_m$, $\tau$ ,and $R_{ds}$.

$$Im(Y11) = j\omega(Cgs + Cgd) \quad (7)$$

$$Im(Y12) = -j\omega(Cgd) \quad (8) \qquad Im(Y21) = gm - j\omega(Cgd) \quad (9)$$

$$Im(Y22) = j\omega(Cds + Cgd) + \frac{1}{Rds} \quad (10)$$

The components' values of the linear model are listed above. In order to show the validity of our model the S-parameters were measured at two different bias voltage (Vgs = 0.6V, $V_{ds}$ = 0.1V and $V_{gs}$ = 1.2V, $V_{ds}$ = 3V) corresponding successively to the linear and saturation regions, figure 3 a-b, show that the models' S-parameters are in a good agreement with the measured data in 0.1-5.1 GHz frequency range. This equivalent small signal linear model can be used to determine a nonlinear MOSFET model.



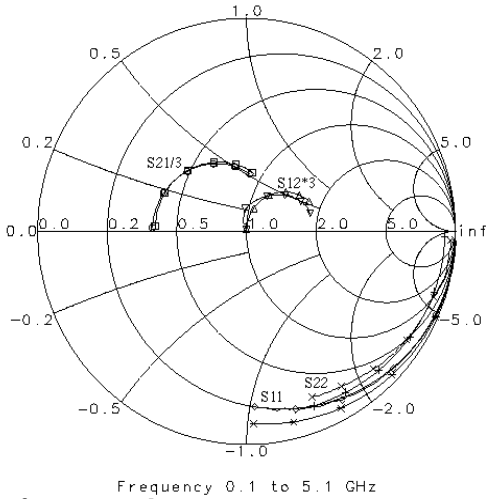




figure 3 a-b S-parameters comparison

**Nonlinear MOSFET transistor.**

A number of nonlinear transistors models have been developed and include equivalent circuits model [7], physical model [8], black box model [9]. Equivalent circuit model can be easily obtained and quickly analysed by nonlinear circuit simulation software.

The extrinsic model remains the same seeing that its elements are independant of the biasing voltage, all the extrinsic elements values who are bias dependant will be modeled, except of Cgs which is considered to be linear fixed capacitor in our detector configuration circuit [7]. The technique used is based on DC and S-parameters measurements.

*DC measurements.*

The voltage controlled current source I-V is the principal nonlinear element of the transistor so, it's representation is a major point in transistor modeling, it has been detemined from DC measurements (I-V characteristic) at Vgs = 0.6V. In order to describe the evolution of the drain current over a large range of drain bias variation, positive and negative current has been measured for the linear and saturation region, the measured data has been fitted with a polynomial equation.

$$Ids = C_0 + C_1 * V_{ds} + C_2 * V_{ds}^2 + \ldots\ldots C_n * V_{ds}^n$$

$C_0$= -26e-5, $C_1$= 41e-4, $C_2$= -16e-4, $C_3$= -55e-4, $C_4$= -25e-4, $C_5$= 10e-3, $C_6$= -43e-4, $C_7$= -98e-5, $C_8$= 89e-5, $C_9$= -13e-5.

The unknown coefficients are determined using the least-squares method. The representation of the voltage controlled current with an analytic function translates only the behavior of the MOSFET drain current. This may have some drawback and, does not take into account some physical phenomenon such as, thermal effect, channel length and saturation velocity but, for our application, the MOSFET is used in the linear region where the above listed phenomenon are irrelevant on the drain current characteristic.

*S-parameters Measurements.*

As stated above the capacitors $C_{gd}$ and $C_{ds}$ are function of the drain voltage across them, several S-parameters measurements at different drain voltage have been achieved to extract the variation of each capacitor in function of the drain voltage. The same method of polynomial equation fitting has been carried out to model the nonlinear capacitors.

**Measurements Results and Discussion.**

Using DC and S-parameters method outlined in the previous section, a linear and nonlinear RF MOSFET model have been extracted and implemented in a circuit simulator LIBRA for model evaluation and, therefore prediction of the RF power detector results. The silicon MMIC circuit has been realized in silicon with MOS technology, its overall size is about $1mm^2$. An automated on wafer measurements have been achieved for different RF power levels at Vgs=0.6V. A comparison has been carried out for both structures [5]. Figure 4, shows a thorough comparison between measurements and predicted output voltage in the 1-2 GHz frequency range, f for the second structure detector design (figure 1b). One can see that the measurements results are generally in agreement with the computed simulations, the poorer agreement occurs around 2 Ghz, this can be largely attributed to the model itself. The voltage control current source and the capacitors equation fitting may affect the predicted results. It is believed that measurements errors can also have a small contributions and the finite isolation between the DC generator and the drain of the MOSFET.

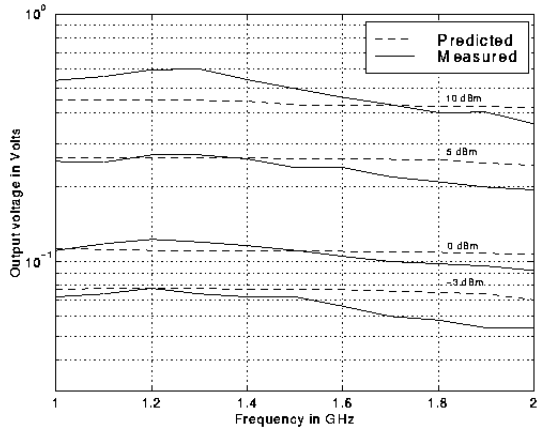



figure 4 predicted and measured results comparison

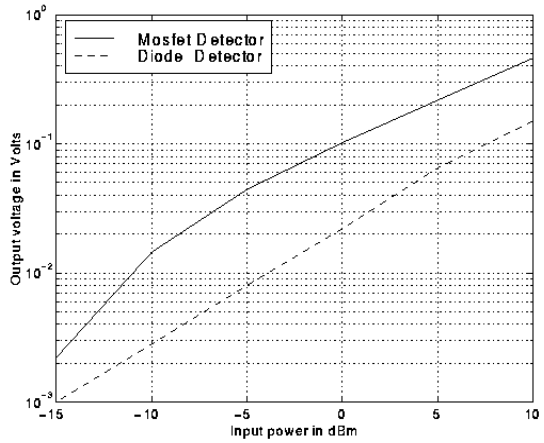



figure 5. MOSFET and Schottky diode output voltage

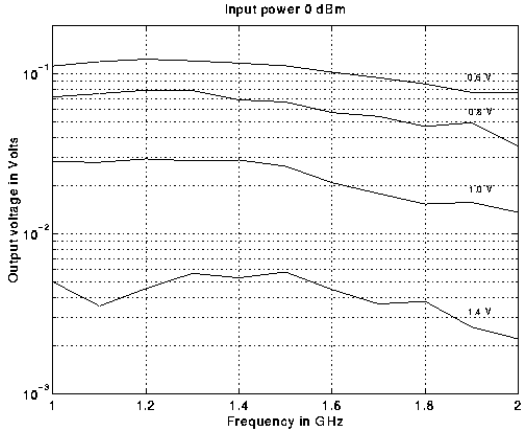



figure 6 Variation of MOSFET detector vs gate bias

Figure 5, shows a comparison between a MOSFET and biased GaAs Schottky diode detector. This detector used a common configuration circuit with a serie diode and a RC filter. The MMIC circuit has been made with GaAs F20 technology by the GEC-MARCONI foundry. The sensitivity of the MOSFET is higher than diode counterpart however, the linearity is for both case the same. Figure 6, shows the variation of MOSFET detector sensitivity with the gate bias voltage. As the gate bias voltage ($V_{gs}$) increases, the I-V nonlinearity characteristic decreases as well as the sensitivity.

**CONCLUSION.**

A novel MMIC RF power detector has been designed using silicon technology. The proposed linear model fits very well practical S-parameters, and the non linear model gives a prediction of the detector's output voltage. The detector is suitable for RF power measurements and features a better sensitivity compared to a biased Schottky diode detector. The output voltage is directly collected at the resistance load, contrary to the diode counterpart, where the bias voltage is added to the output voltage. Field effect transistors are less sensitive to temperature variations than Schottky diodes, all this makes the silicon MOSFET detectors major player in the RF power measurements.

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